Interconnect (beol) (PEX)

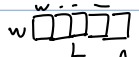
C, R, L

Know where to do extraction, and what (R, L)

C ~ fF/μm

R Ω/square (sheet resistivity) $R = \frac{\rho L}{wt} = \frac{\rho}{t} \cdot \frac{L}{w}$ (ohm per square of width w)

(ρ: Ω·cm; $\frac{\rho}{t}$: sheet resistivity)



lower (thinner) ~0.03 Ω/□ higher ↓

L ~10nH/mm

Cu, Au contaminates Si → deposit diffusion barrier

ILD (inter layer dielectric) lower ε than SiO_2

Scaling by $\frac{1}{s}$ on w, t, spacing, s_L on L

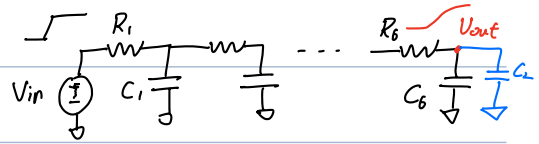
$C \sim \frac{A}{d}$ (parallel plate) $= \frac{1/s \; s_L}{1/s} = s_L$ (neighbor)

$R \sim \frac{L}{wt} = \frac{s_L}{1/s \; 1/s} = s^2 s_L$ ↑↑

1. $RC \sim s^2 s_L^2$ (=1 if $s_L = \frac{1}{s}$, but $s_L \sim 1$ since more transistors → $\sim s^2$)

point-2-point net (no fanout, C goes to gnd)

n-pole LPF → delay & slew



Approx: Elmore delay (single-pole approx (Padé) of multipole sys. (not dominant pole))

$$\tau = \overbrace{R_1 C_1 + (R_1 + R_2) C_2 + \cdots + (R_1 + \cdots + R_6) C_6}^{\text{intrinsic}} + \overbrace{(R_1 + \cdots + R_6) C_L}^{\text{extrinsic}}$$

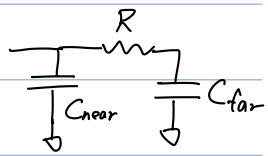
when? to analyze? No for short wire. Just extract C.

Compare τ against slew rate (~FO4)

2. Resistive shielding

Suppose driver slewed fast. Can't see the line cap, since slew much faster

When sizing driver, $C_{eff} < C_{actual}$, since part shielded by line RC



Model C_{near}, C_{far}, R → π model

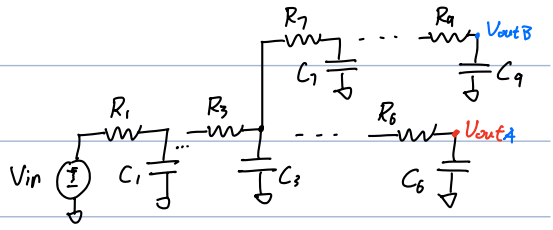
$C_{total} = C_{near} + C_{far}$

driver only sees C_{near}, C_{far} sheilded by $R C_{far}$

Fanout gets total branch cap.

$T_A = \cdots + (R_1+R_2+R_3)(C_3+C_7+C_8+C_9) + \cdots$

$T_B = \cdots + \text{--} (C_3+C_4+C_5+C_6) + \cdots$



Fix large RC

1. Repeater → buffer delay, need via M_{high} to SUB, hard to floorplan, power
2. wider wire → R↓ (good for extrinsic), but C↑

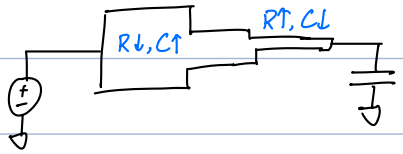
   C has 1. areal $\sim w^1$

   2. fringe unchanged → also good

:(area, power ↑ due to C↑

Wired tapering (R_{near} ↓, wide to narrow)

less aggregated C → :)



E. wire, 1mm long, 0.4μ width, 0.1fF/μm, 0.076Ω/□, 500 fF loading

If wire is purely distributed, $\mathcal{R}$, $\mathcal{C}$ (R/L, C/L), $T_{elm} = \frac{1}{2} R_{tot} C_{tot} = \frac{1}{2} \mathcal{R} \mathcal{C} L^2$ (avg. $R = \frac{R}{2}$)

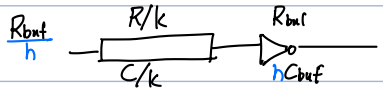
$= \frac{1}{2} \cdot (0.076 \cdot \frac{1mm}{0.4\mu m})(0.1 \frac{fF}{\mu m} \cdot 1mm)$

$= 9.5\,ps$

$T_{ext} = R_{tot} C_L = \frac{1}{2}(0.076 \cdot \frac{1000}{0.4}) \cdot 500\,fF = 95\,ps$ → dominant

Sln. 1. widen (taper) wire

✓ 2. Add repeaters (breaks L^2) #? size?



break into k same segments (not, but close to optimal)

Let repeater have R_{buf}, C_{buf}, xh

$T = k[T_{int} + T_{ext} + T_{buf}]$

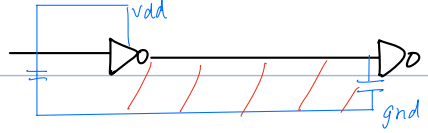
$= k\left[\frac{1}{2}\frac{RC}{k^2} + \frac{R}{k} h C_{buf} + \left(\frac{R_{buf}}{h} + \frac{R}{k}\right)\left(\frac{C}{k} + h C_{buf}\right)\right]$ (ignore R shielding)

$\frac{\partial T}{\partial h} = R C_{buf} - \frac{R_{buf} C}{h^2} = 0$

$h = \sqrt{\frac{R_{buf} C}{R C_{buf}}}$

$\frac{\partial T}{\partial k} = -\frac{RC}{2k^2} + R_{buf} C_{buf} = 0$

$k = \sqrt{\frac{\frac{1}{2}RC}{R_{buf} C_{buf}}} = \sqrt{\frac{T_{intrinsic}}{D_0\ cost}}$

L. 

charges C via I_{disp}, through gnd–vdd loop

$V = \frac{\partial \Phi}{dt} = L\frac{dI}{dt}$, L depends on the loop. Loop depends on f (minimize $R + j\omega L$) @ hi f, find lower L path

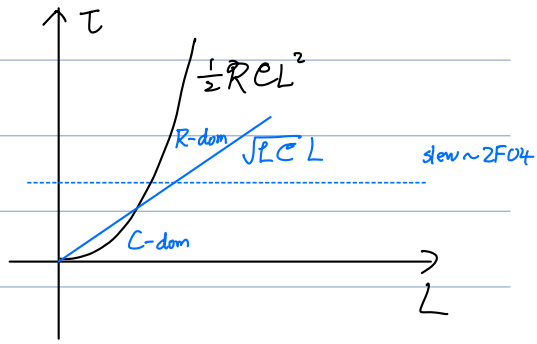
@ high f, find low L path (smaller Φ, smaller A)

E. if vdd/gnd path near → return via decoupling C → good, predictable. E. p/g planes in PCB

If return via signal line, :(

Extraction: assume proximity of vdd/g lines.

When to care? $\sqrt{LC}L$ curve (speed of light)

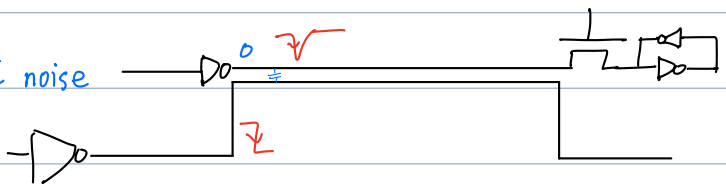


For all delays > slew, mainly R, L don't care

→ 3μm, Cu interconnect → R↓

tech → FO4↓ → L matters more

If $\sqrt{LC}$ dom. → like transmission line, may have ringing if Z not matched

CC noise 

if aggressor pulls below gnd → $V_{GS} > 0$ → pt on → X

Always add Do at pt input.

Delay if 2 nets switch opposite, C_C sees Miller eff. (2x I_{disp}), $C_{eq} = 2C_C$

if switch same, $C_{eq} = 0$ → early mode problem

Power net, integrity (IR drop (DC);

1. IR drop: pulling I thru R_{supply}
2. AC $L\frac{dI}{dt}$ noise, ΔI noise, simultaneous switching

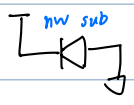
Grid, sotter balls → center

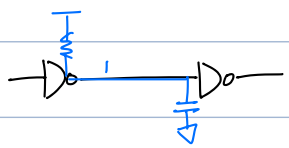
Add pre-charged decoupling C caps, after supply L. Distributed over chip

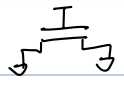
Cimplicit: 1. p/g cap between M, low R shielding

2. Nwell–substrate cap (RB pnj), R shielded

3. non-switching Do (heavily shielded)





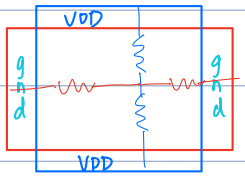
Cexplicit: Add deCap → 

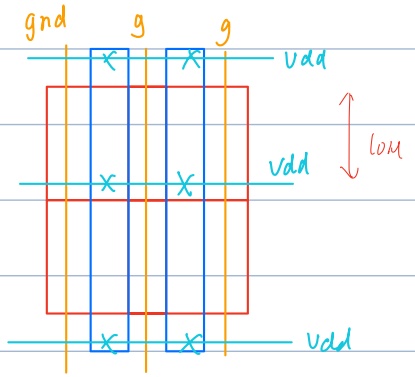
Distribute at >5V : IVR (integrated voltage regulator) (DC→DC)

Decap What's total C from clk in FF $\xrightarrow{\times 10}$ decap

Use a large M → C comes w/ high series R → shielded :(

↳ array of smaller devices





LC resonance ($\frac{1}{10}$ clk freq). Need Q↓

Clocking sync, async

GALS (globally async locally sync) E. multicore processor

Sync. clk distribution

Metric 1. Skew (DC, static Δt)

2. Jitter (period), caused by supply noise

3. Power

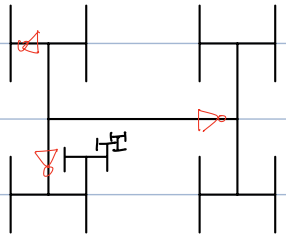
4. Latency (delay from src to sink) Latency amplifies jitter caused by supply noise

skew/

1. Tree (modified H-tree), recursive

✓ Spare in use of interconnect

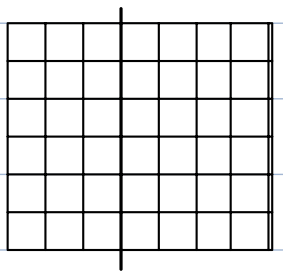
X Sensitive to loading. Need adjust w/ buffers (need to tune)



2. Grid, driven by a very large transistor (~cm)

✓ Low L, R. Insensitive to loading

X outside skews, high C, lots of wire



Tree-driver grid. Tree drives a less dense grid

✓ No dense wires, good loading

Active deskewing solves skew & jitter

Use programmable delay line (prog. after fab)

Packaging Interconnect Protect Heat out

MCM Multi-chip module

SoC Make bigger chip, use its interconnect network to provide density

issue stuck w/ one technology

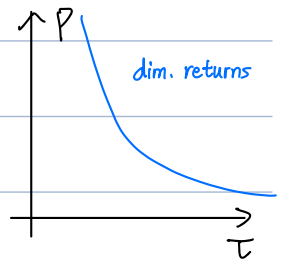
design reuse : IP

yield (big chip)

COWOS (chip on wafer on substrate)

Low power (wasted on unused (dark Si)

easy
1. clk stuff that's unused → clk gating
2. leakage on dark → gate Vdd w/ large, high V_T (no leak itself) device
3. energy-delay tradeoff → peruto curve



Knob: Vdd → DVFS (dyn. voltage & freq. scaling) based on workload

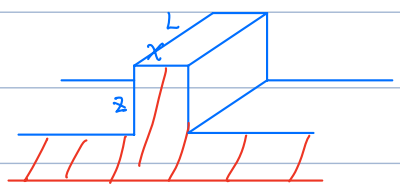
need dc-dc converter 1. linear var. reg

2. sw. cap./ind. converter

Finfet : bulk cmos ugly at 22nm → very short channel,

subthresh slope bad (>100 mV/dec)

poor electrostatics



finfet gates at multiple sides

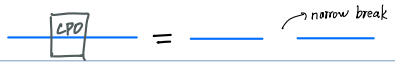
Weff = w + 2z

widths quantized by # of fins

Co changed to new layer: MD (MD) OD, MP (MP) PO → use via 0 to contact M1

body plug : detatched body, connected MD (MP) MD

cmd (cut md), cpo (cut poly) → make break in md/po, but reduce spacing



Fin boundary follow fin grid

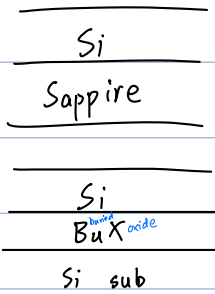
PODE (poly on OD edge) OD on poly (pode) OD, mark dummy, extracted, but lvs not compared, 3T dev (~1 s/d)

Bulk CMOS 3-layer PW → NW → diff

Silicon on Sapphire cosmic ray → soft error

ionization does not generate EHP in sappire insulator

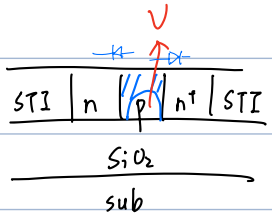
S O I → Insulator

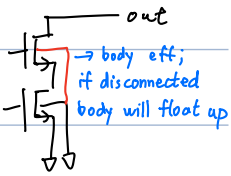


PD-SOI (partially depleted) no depletion region $C_{s,o}$ ↓

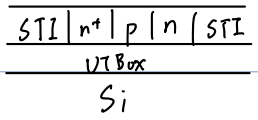
part is still neutral → has a floating (body) potential

but helps by V_T↑, reduces body effect in stacks





FD-SOI (fully depleted) (UTB) (ultrathin body) thin → no body → 3-terminal

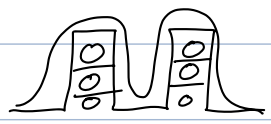


V_T very sensitive to Si thickness

Can use Si underneath to backgate → tune V_T (ana. V_B control)

Finfet (3 sides)

GAA gate all around (4 sides)



Wires Backside power

TSV thru Si via, access back side for power distribution

ROM (also for flash (non-volatile))

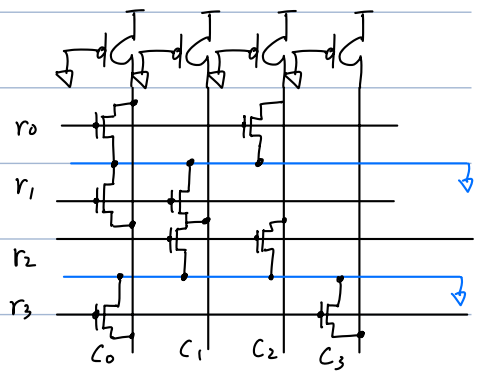
store → microcode

CISC → subroutine converts to RISC

Floating gate (neg. leakage), but write limit

1. nor pseudo-nmos

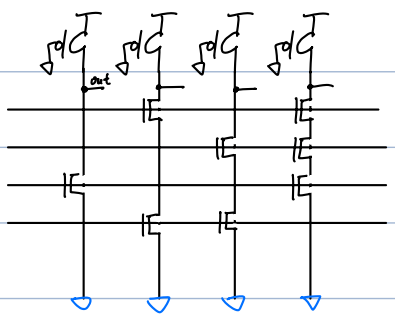
R (one-hot)	C_1	C_2	C_3	C_4
1	0	1	0	1
2	0	0	1	1
3	1	0	0	1
4	0	1	1	0



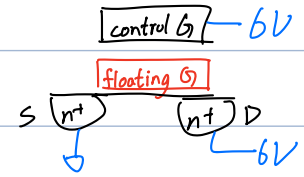
2. nand

more dense, but slower (stack)

power w/ one-cold rows, same table (opposite placement



EPROM



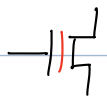
Floating G changes V_t, so won't be turned on.

W Apply ~6V to control and S-D → Fowler-Nordhein

e^- tunnel from inv. layer → trapped in floating gate.

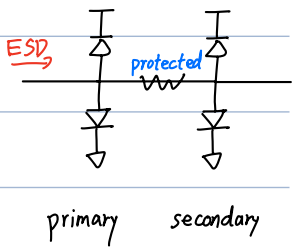
Erase old UV erase

new E^2PROM (electrically erasable) Put 12V @ S, 0V @ C, float D → erase



Need DC-DC for large voltage

ESD



1. Human body model (effect of human touch)
2. CBM

Diodes turn on to drain ESD (in IO cells)

Issue diode large C → RC problem