Digital Electronics Lab 3 Report

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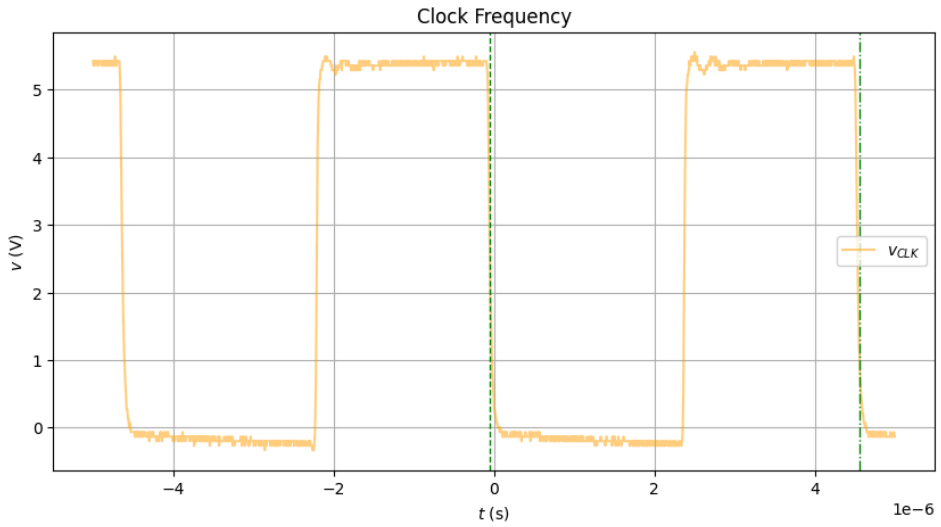
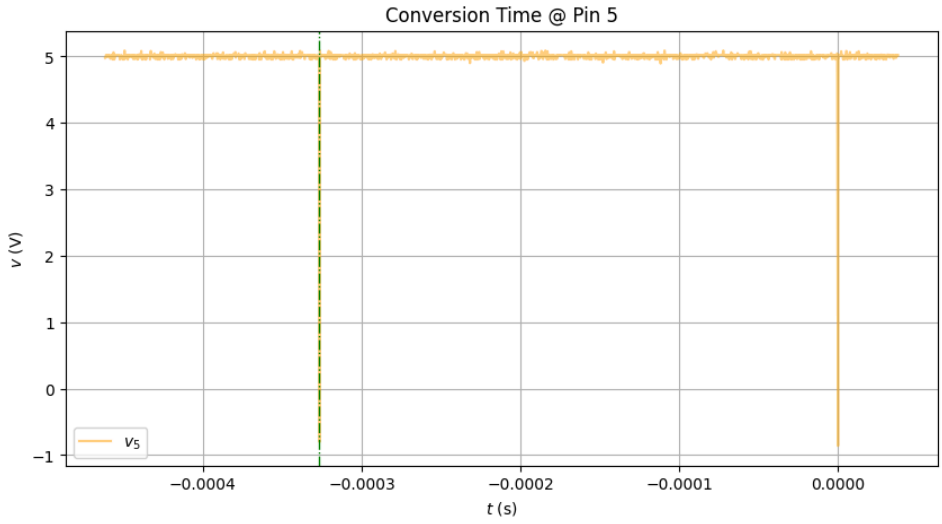
ADC

Q1 Clock Frequency



$f = 1/(t_2 - t_1) = 1/(4.55e\text{-}6\ s - 6e\text{-}8\ s) = 223\ kHz$
The clock frequency at pin 19 is about 223 kHz.

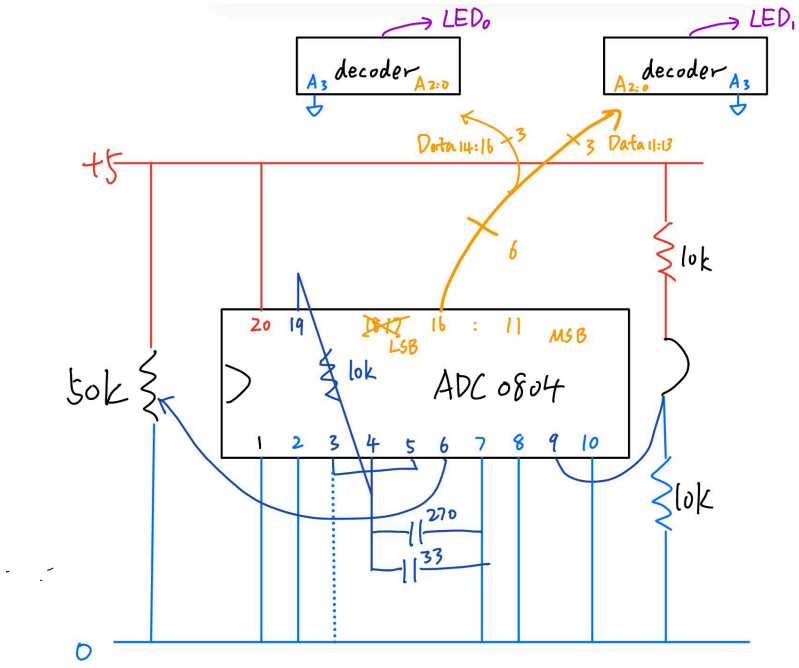


We observed the period between two peaks at pin 5 (INTR), signaling conversions.
$T_{conversion}$ = 0 s - (-3.27e-4 s) = 327 us.
327 us / (1/223 kHz) = 72.92, approximately 73 clock cycles.
We tested for various input voltages. The conversion time was independent of the input voltage.

D1 Voltmeter

We kept the ADC design for Q1 and modified it as follows:

- Input pin 6 is connected to a pot such that V_{in+} can be varied from 0V to 5V.
- For the DATA pins, we use two groups of three digits of the output of ADC where each group can produce one octal representation as (2^3 =8). We took the 3 MSBs ($DATA_{11:13}$) to the MSB of a 7-seg decoder and LED (LED_1), and $DATA_{14:16}$ to the LSB of the 7-seg decoder and LED (LED_0). The 2 LSBs from the ADC ($DATA_{17:18}$) are unused.
- Next, HCF4511B (BCD to SEVEN Segment Latch) is used to convert each group of octal representation to 7 inputs of the LED being used. The 7-seg decoders are wired regularly, except that the inputs' MSBs (pin 6) are grounded. The decoder outputs are then fed into the LEDs. We used an additional voltmeter to track the input to ADC.



Below are the results. The input ranges from [0, 5], and the octal output ranges from [0, 63_{10}]. Therefore, V_{out} = LED_{10} * 5/63

V_{in} (V)	$Output_8$	$Output_{10}$	Expected out_{10}	$Error_{10}$	Error (V)
0.00	00	0	0	0	0
0.59	10	8	7.434	0.566	0.04
1.82	27	23	22.932	0.068	0.01
2.81	44	36	35.406	0.594	0.05
5	77	63	63	0	0

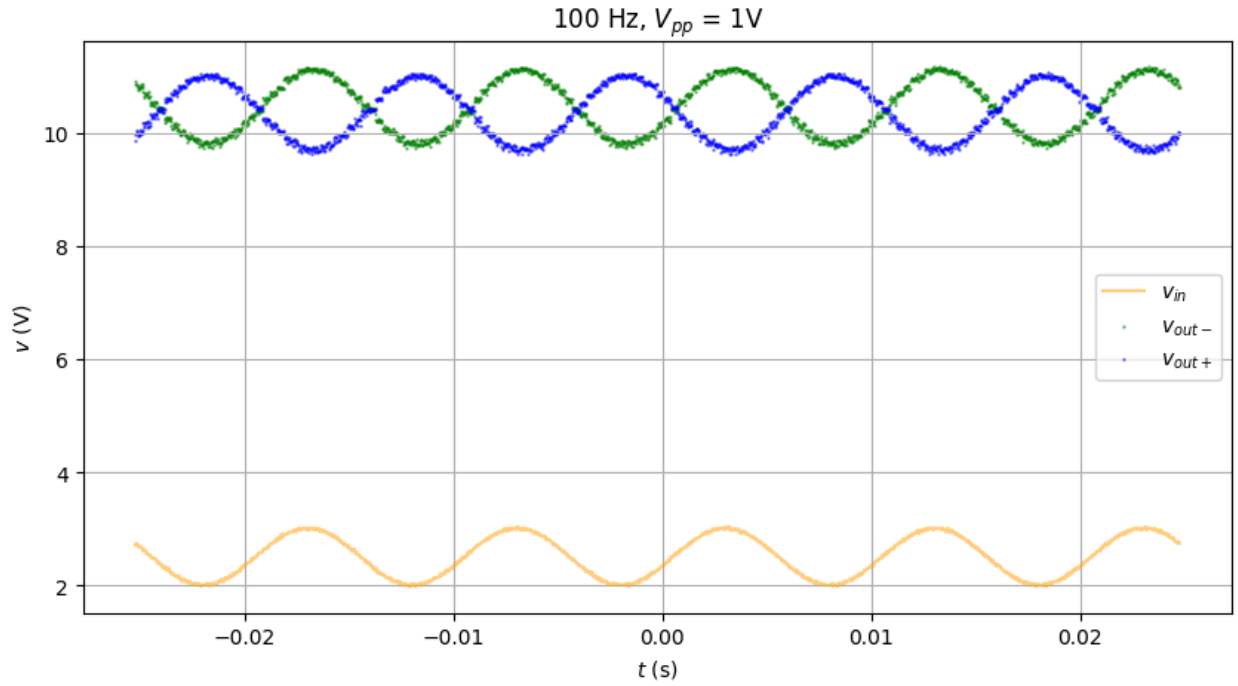
The converted output voltage is correct. The errors are tiny

DAC

Theory

We constructed the circuit as suggested, and fed a 100 Hz, $1V_{pp}$ sine wave with +2.5 V offset.

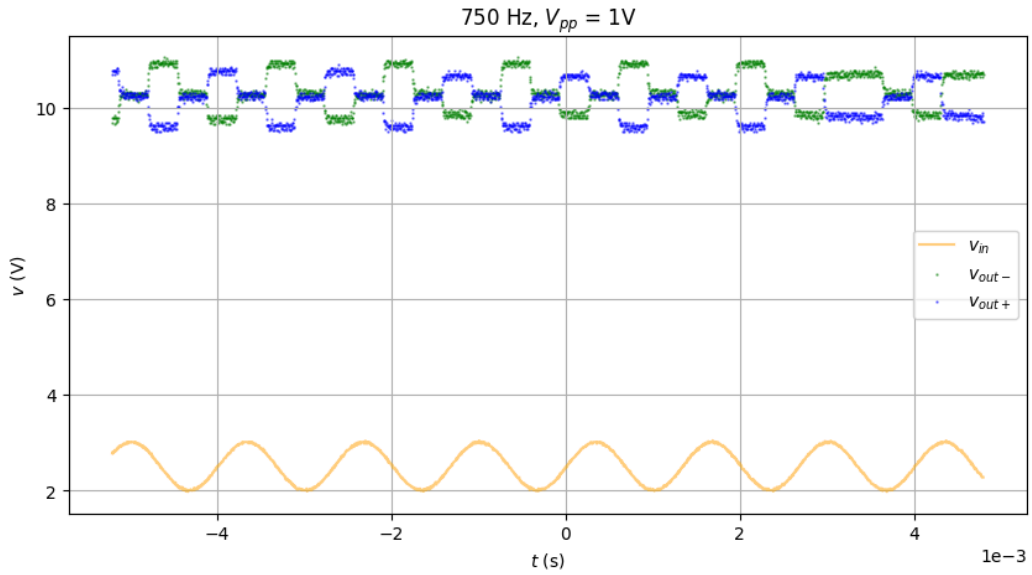
We observed sinusoidal behavior at the outputs, as expected, but the output amplitude was too small. We then replaced the 10k resistors at I_{out+} and I_{out-} to 100k to pull down more voltage. DAC takes in a digital signal, transforms it via a bias network, and applies it on BJTs to output multiple levels of output *currents*. The characteristic transconductance (i.e. the gain) of DAC thus depends on the output load resistance and whether or not the compliment gain of the op amp inside DAC is turned on or not. With higher load resistance, the gain is larger.



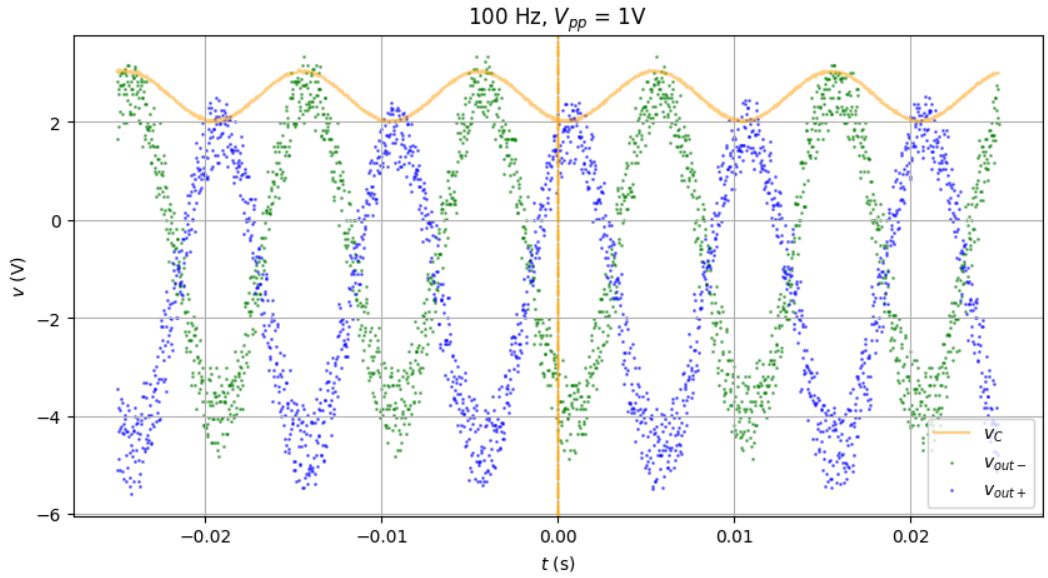
As the digital input at DATA increases, I_{out+} increases while I_{out-} decreases. An increasing output current will pull down the output voltages. Therefore, V_{out+} (blue) has an inverting phase, while V_{out-} (green)'s phase is not inverted.
Even with 100k output load, the output amplitudes are still tiny, though, suggesting a problem within the DAC's current source amplifier
The output swings are:
V_{out-}: 9.80 V - 11.15 V
V_{out+}: 9.65 V - 11.05 V

Q2a Aliasing

By the Nyquist Sampling theorem, we should be able to recover the signal if the sampling frequency is at least twice the signal's bandwidth. Our ADC sampling period is about 327 us (3.06 kHz). The Nyquist frequency is half the sampling frequency: 1.53 kHz.
We observed the output at 750 Hz, which is below the Nyquist frequency
The result was not expected: the output waveforms are aliased with low-frequency components. Evidence of aliasing begins before the expected frequency.

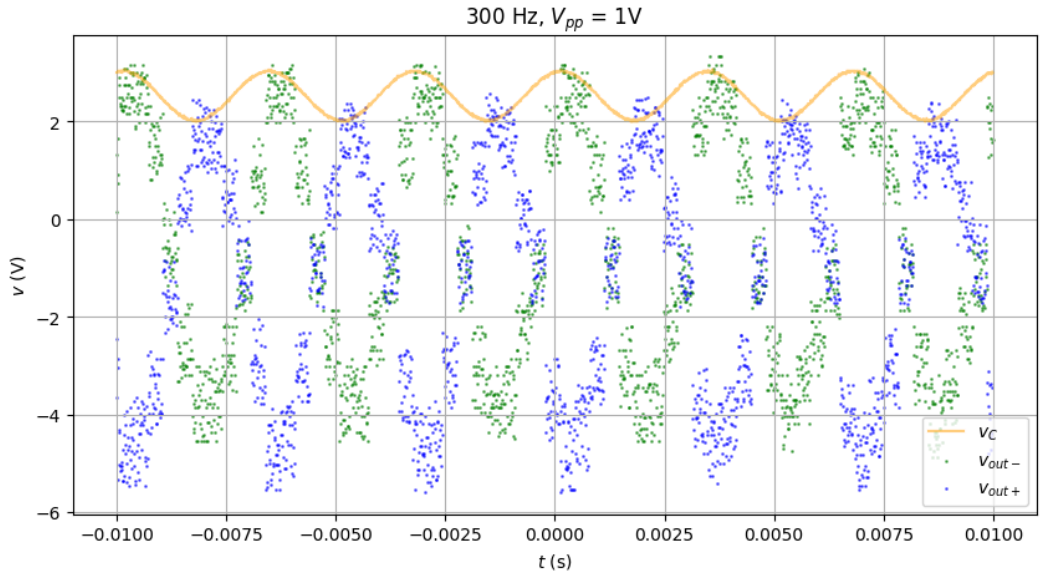


Because our DAC has amplification issues, we used the DAC from Charlie and Millie after they were done, and took separate measurements with the regular 10k output loads.



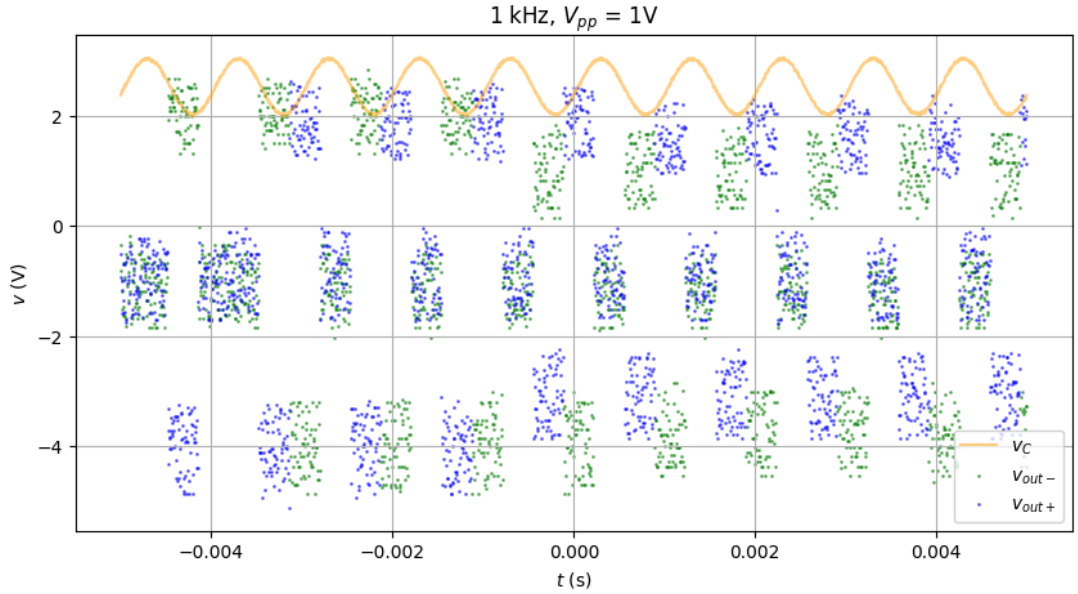
100 Hz Output range:
V_{out-}: -4.7 V - 3.3 V
V_{out+}: -5.5 V - 2.5 V

We then increased the frequency slightly, to 300 Hz.



At 300 Hz, the output waveform began to look distorted,

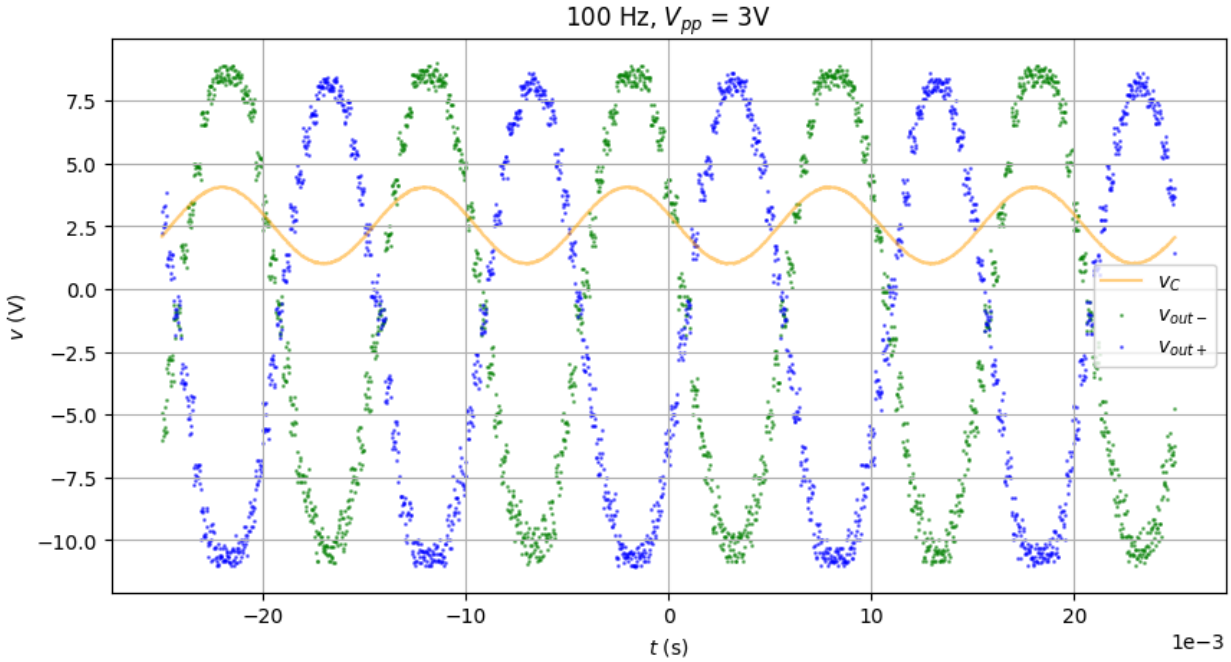
We increased the frequency to 1 kHz, slightly smaller than the Nyquist frequency of 1.53 kHz. However, significant aliasing is present. We can clearly see the 1 kHz component, but the whole sine wave is encapsulated inside a larger envelope with a much lower frequency.

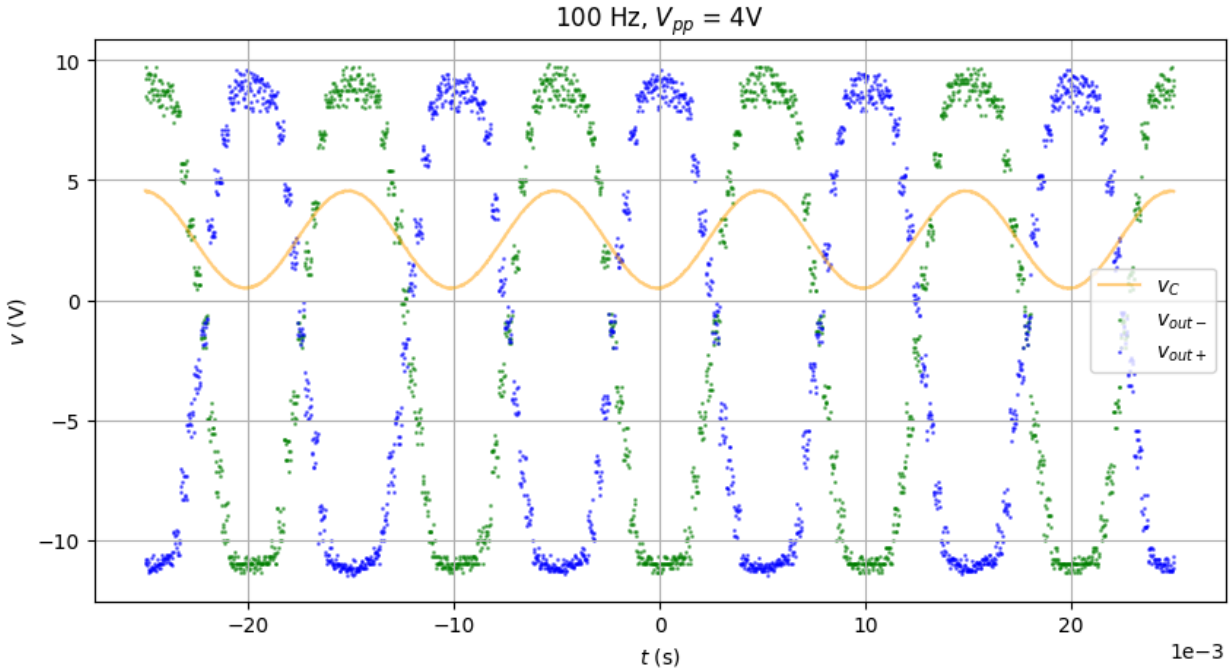


Theoretically, we should be able to recover the signal with ADC/DAC up to a bandwidth of 1.53 kHz. However, due to nonideality (white Gaussian noise for example), the upper limit of the bandwidth of the recoverable signal is much smaller than expected.
To transform it back to fully analog signals, we need further mathematical manipulations, for example, sinc interpolation functions

Q2b Input Amplitude

We used Charlie and Millie's DAC to measure with different input amplitude values.





As the input amplitude increases, the output voltage swing rises proportionally.
The output waveform looks fine at V_{pp} = 3V at input, but distorted at V_{pp} = 4 V. This is because inside, the DAC transistor output voltage swing is reached. Beyond that, the transistors will no longer be in the active mode. Therefore, the outputs are capped.