Digital Electronics Lab 2 Report

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Q1. Astable

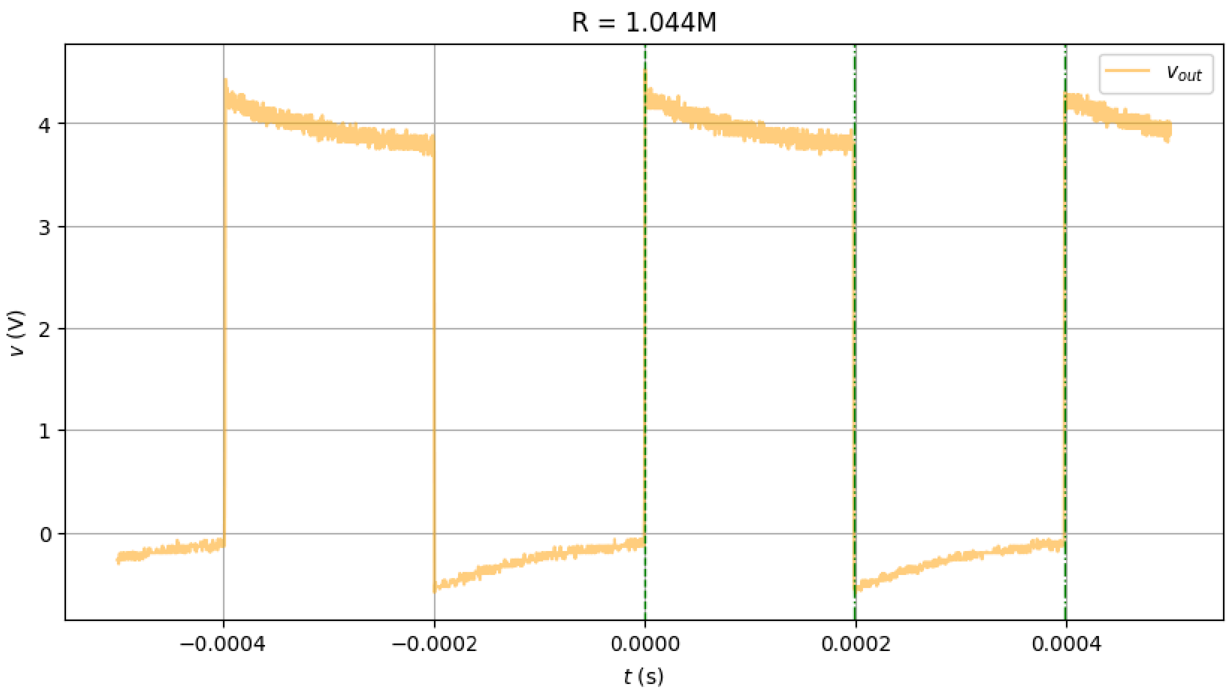
- C charges via R_1 and R_2 from ⅓ V_{CC} to ⅔ V_{CC}. The time constant is $(R_1 + R_2)C$
  $T_{rise} = (\ln(⅔V_{CC}) - \ln(⅓V_{CC}))\ (R_1 + R_2)C = \ln(2)\ (R_1 + R_2)\ C$.

- C discharges via R_2 only, from ⅔ V_{CC} to ⅓ V_{CC}. Through a similar logic, $T_{fall} = \ln(2)\ R_2C$
- $f = \frac{1}{T_{rise}+T_{fall}} = \frac{1}{ln(2)\ (R_1+2R_2)C}$
- Duty cycle $= \frac{T_{rise}}{T_{fall}} = \frac{R_1+R_2}{R_2}$

We used a pot to vary R_2 from 1.044 MΩ to 2.2 kΩ.

R_2 = 1.044 MΩ

This is the maximum value of the R_2 pot.



t_H = 1.99e-4 s - 0 s = 199 µs
t_L = 3.98e-4 s - 1.99e-4 s = 199 us
T = 3.98e-4 s - 0 s = 398 us
F = 1/T = 2.51 kHz
Duty cycle = 199 us / 398 us = 50%

In[5]:= $R1 = 2.2\times10^{3};$ (*Ω*)
$R2 = 1.044\times10^{6};$ (*Ω*)
$Ca = 270\times10^{-12};$ (*F*)

In[8]:= $f = \frac{1}{(R1 + 2\,R2)\;Ca\;Log[2]}$ (*Hz*)

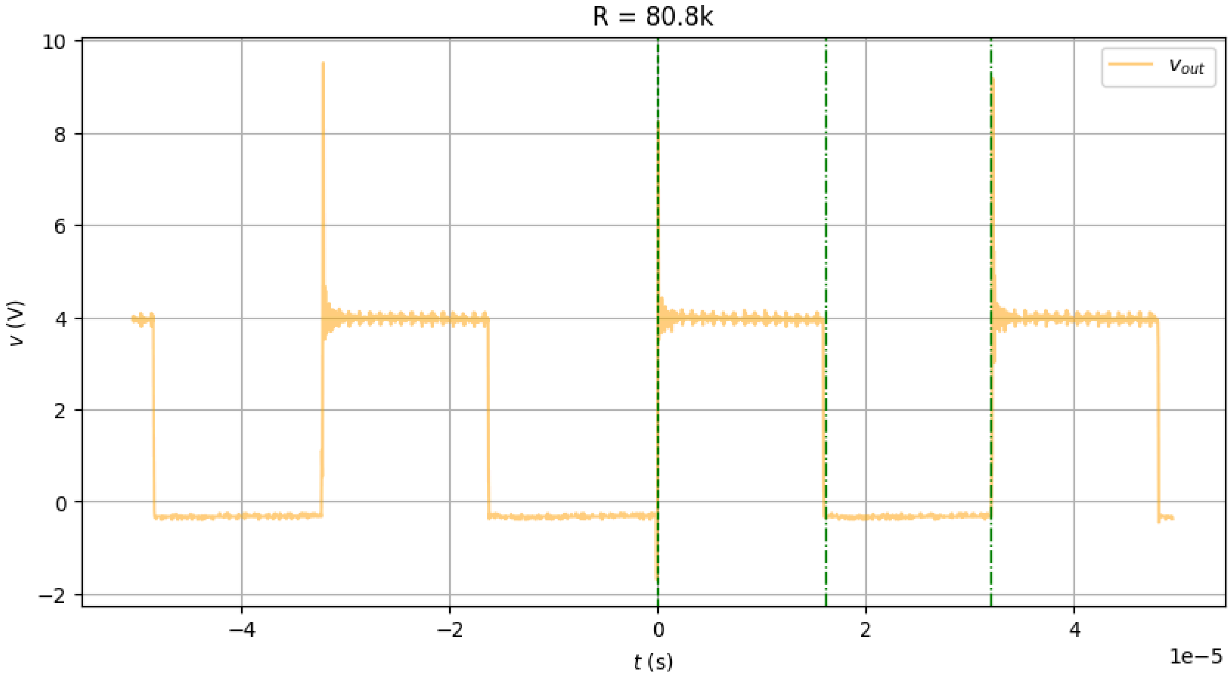
Out[8]= 2556.37

In[13]:= $thigh = (R1 + R2)\;Ca\;Log[2];$
$tlow = R2\;Ca\;Log[2];$
$dutycycle = \frac{thigh}{thigh + tlow}\,100$ (*%*)

Out[15]= 50.0526

Theoretically, we have frequency = 2.56 kHz and duty cycle = 50.1%. The measured and the theoretical values agree to the first decimal place.

R_2 = 80.8 kΩ



T_H = 1.61e-5 s - 0 s = 16.1 us
T_L = 3.2e-5 s - 1.61e-5 s = 15.9 us
T = 3.2 e-5 s - 0 s = 32.0 us
f = 1/T = 31.3 kHz
Duty cycle = 16.1 us / 32.0 us = 50.3%

In[18]:= R1 = 2.2×10^3; (*Ω*)
R2 = 80.8×10^3; (*Ω*)
Ca = 270×10^{-12}; (*F*)

In[20]:= $f = \frac{1}{(R1 + 2\,R2)\,Ca\,Log[2]}$ (*Hz*)

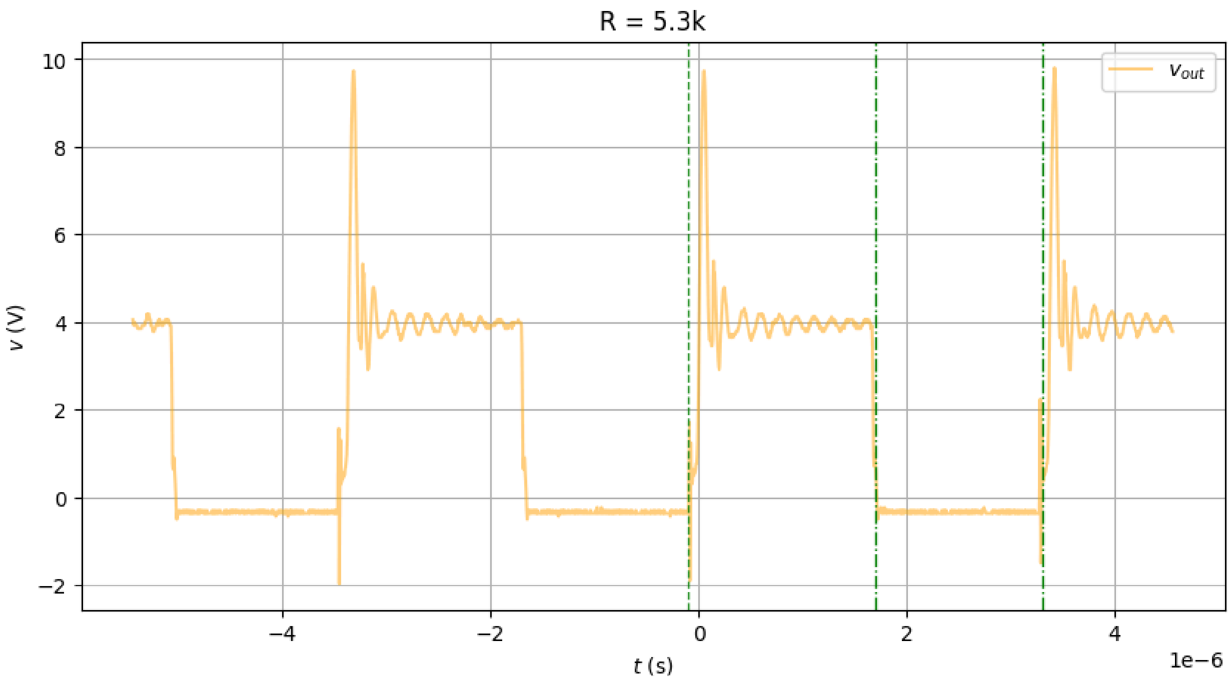
Out[20]= 32 621.

In[21]:= thigh = (R1 + R2) Ca Log[2];
tlow = R2 Ca Log[2];
$dutycycle = \frac{thigh}{thigh + tlow}\,100$ (*%*)

Out[23]= 50.6716

Theoretically, we expect the frequency to be 32.6 kHz and the duty cycle to be 50.7%. The theoretical values are slightly larger than the measured values.

R_2 = 5.3 kΩ



T_H = 1.7e-6 s + 0.1e-6 s= 1.8 us
T_L = 3.3e-6s - 1.7e-6 s = 1.6 us
T = 3.3e-6s + 0.1e-6s = 3.4 us
f = 1/T = 294 kHz
Duty cycle = 1.8 us / 3.4 us = 52.9%

In[24]:= R1 = 2.2 × 10^3; (*Ω*)
R2 = 5.3 × 10^3; (*Ω*)
Ca = 270 × 10^{-12}; (*F*)

In[26]:= $f = \frac{1}{(R1 + 2\,R2)\ Ca\ Log[2]}$ (*Hz*)

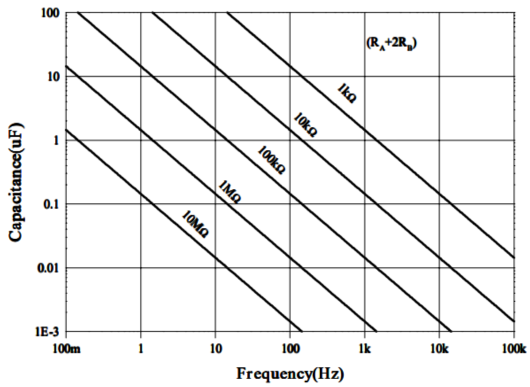
Out[26]= 417 446.

In[27]:= thigh = (R1 + R2) Ca Log[2];
tlow = R2 Ca Log[2];
$dutycycle = \frac{thigh}{thigh + tlow}\ 100$ (*%*)

Out[29]= 58.5938

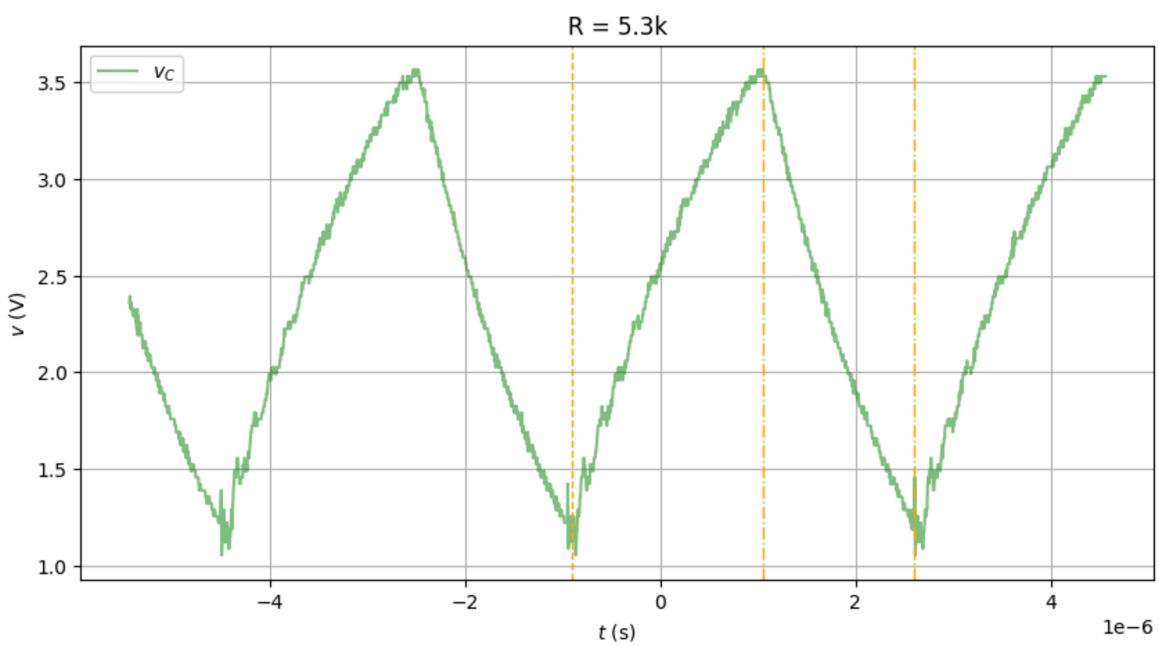
Theoretically, we expect the frequency to be 417 kHz and the duty cycle to be 58.6%. The measured frequency is much less than the theoretical values. The actual duty cycle is also less.

From here, the measured frequency starts to deviate from the theoretical value. Our Fairchild 555 datasheet does not specify a maximum frequency, but Figure 6 in the datasheet only shows frequencies up to 100 kHz. We may be approaching the 555's maximum frequency, and its performance starts to deviate from ideal.
We also observe a large overshoot in the rising edge of the output. This is due to the 100 ns output rising time of the 555.



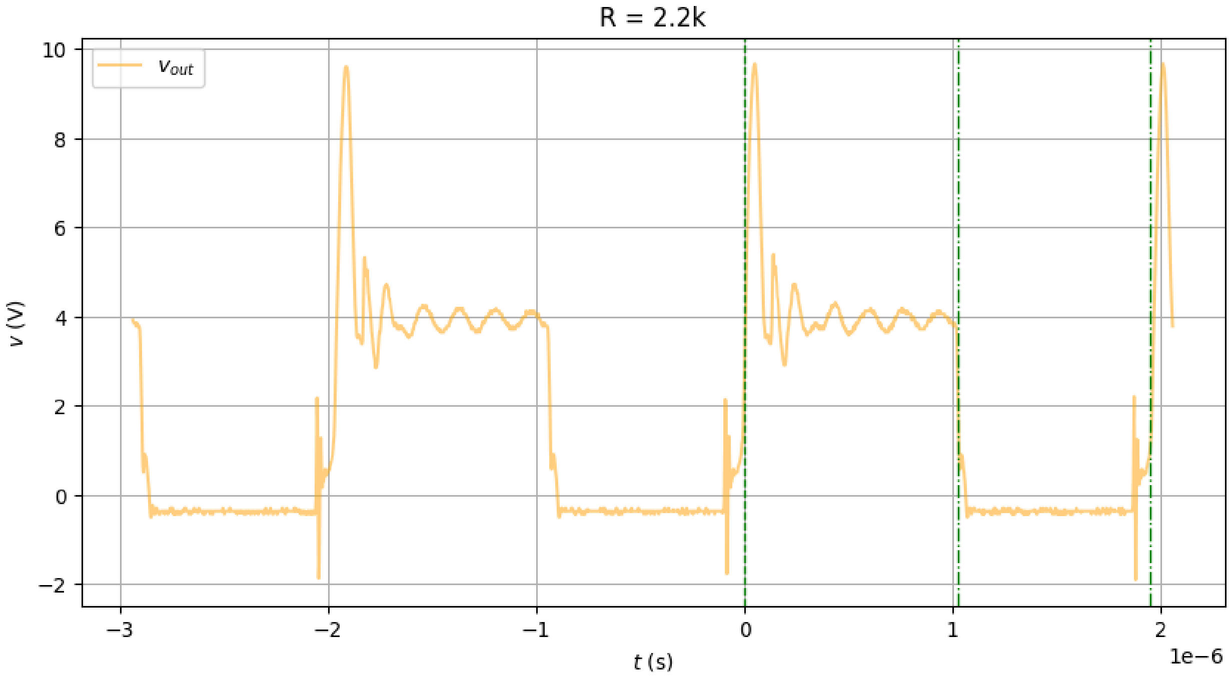
Rise Time of Output (Note4)	tR	-	-	100	-	ns
Fall Time of Output (Note4)	tF	-	-	100	-	ns

Additionally, we measured the capacitor voltage v_C to observe the charging/discharging behavior in more detail.
Duty cycle = (1.05 us + 0.9 us) / (2.6 us + 0.9 us) = 55.7%, which is closer to the theoretical value.



R_2 = 2.2 kΩ

This is the minimum value of R_2 from the pot.



T_H = 1.025 us - 0 us = 1.025 us
T_L = 1.95 us - 1.025 us = 0.925 us
T = 1.95 us - 0 us = 1.95 us
f = 1/T = 512.8 kHz
Duty cycle = 1.025 us / 1.95 us = 52.6%

Again, very poor performance. The output waveform has huge overshoots.

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In[30]:= R1 = 2.2×10^3; (*Ω*)
         R2 = 2.2×10^3; (*Ω*)
         Ca = 270×10^-12; (*F*)

In[32]:= f = 1/((R1 + 2 R2) Ca Log[2]) (*Hz*)

Out[32]= 809593.

In[33]:= thigh = (R1 + R2) Ca Log[2];
         tlow = R2 Ca Log[2];
         dutycycle = thigh/(thigh + tlow) 100 (*%*)

Out[35]= 66.6667
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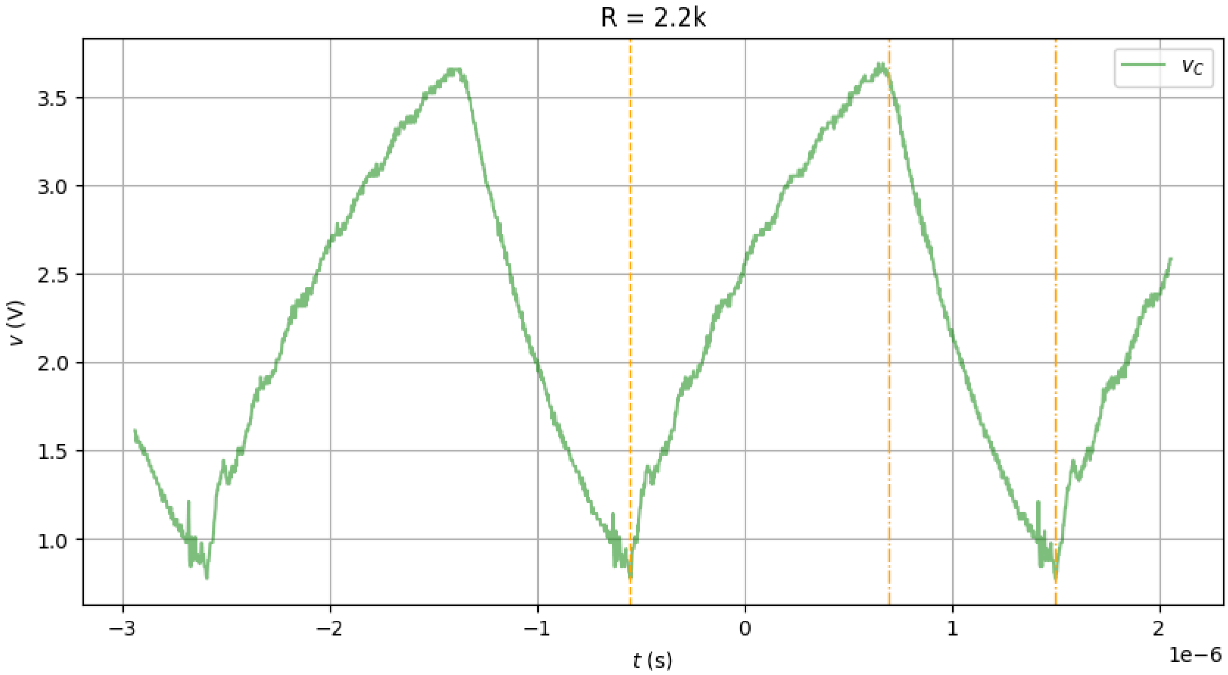
Theoretically, we expect the frequency to be 810 kHz and the duty cycle to be 66.7%. Both the theoretical frequencies and duty cycle are much larger than the measured values. Very poor performance at high frequencies.

Again, we looked at V_C for the charging/discharging pattern.



Duty cycle = (0.7 us + 0.55 us) / (1.5 us + 0.55 us) = 61.0%
Although not perfect, the capacitor's charge/discharge pattern is closer to the theoretical values. You can clearly see the asymmetrical pattern.

Q2. Monostable

Theory

- When trigger (2) stays high, R = 0, S = 0. The system will hold its current state.
- When trigger turns low, S = 1, Q = 1. The discharge transistor is shut down, and the capacitor is charged by V_{CC}.
- When V_C (6) goes above $V_{control}$ (5, ⅔ V_{CC}), R = 1. When the button is released, S = 0, and Q = 0, thus turning on the discharge transistor.
- As V_C discharges below ⅔ V_{CC}, R = 0, S = 0, so Q will hold, discharging the capacitor (very quickly to zero voltage).
- Since there is no return path from the capacitor to trigger, the circuit will not keep oscillating. It will hold Q = 0 until the next trigger.

The capacitor equation after triggering is thus:

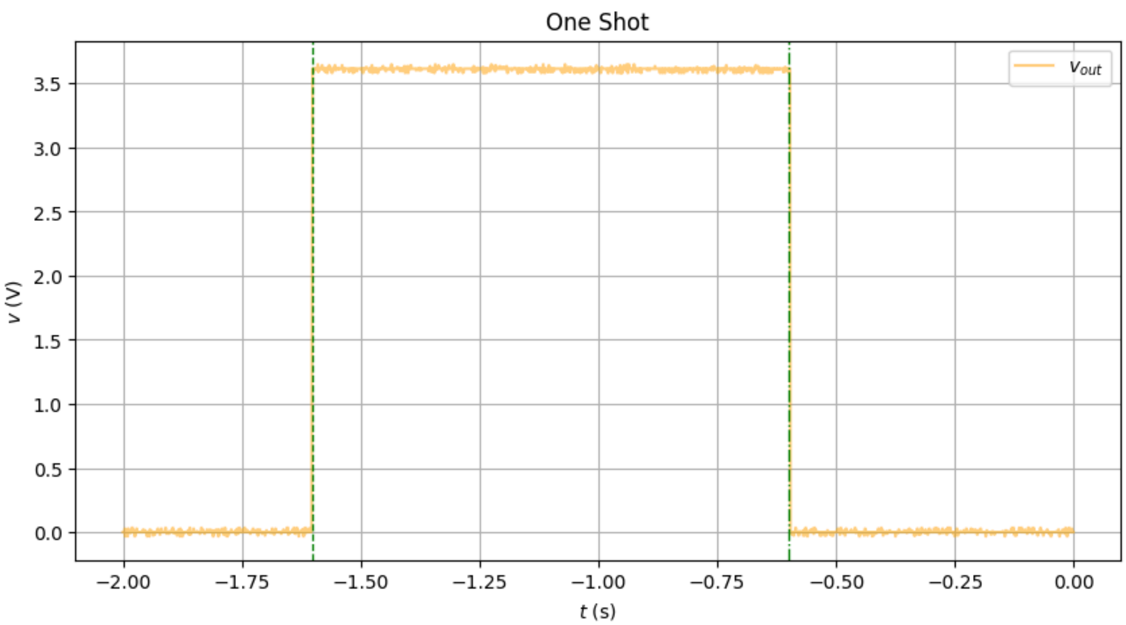
$$v(t) = V_{CC}(1 - e^{-t/(RC)})$$

The duration at which the capacitor charges from 0 to ⅔ V_{cc} is the time that Q is high, i.e. the pulse duration, solving v(t) = ⅔ V_{CC}, we yield: T_{pulse} = ln(3) RC.

Experiment

We initially chose R = (510k + 430k) = 940 kΩ, C = 1 μF.
This should produce t = ln(3) RC = 1.03 s. The actual result was slightly longer than 1 s.

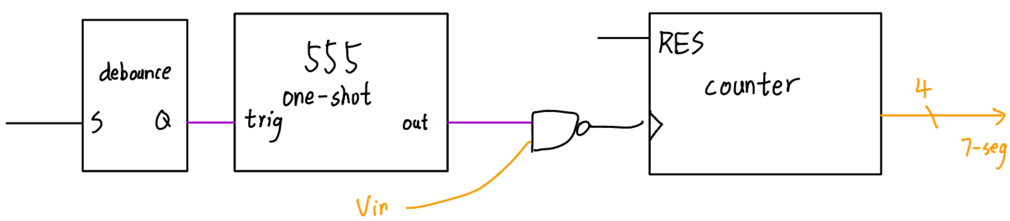
We then chose R = (510k + 300k + 60.4k) = 870.4 kΩ, C = 1 μF.
This should produce t = ln(3) RC = 0.96 s
Experimentally, the duration is almost exactly 1 second. Perfect.



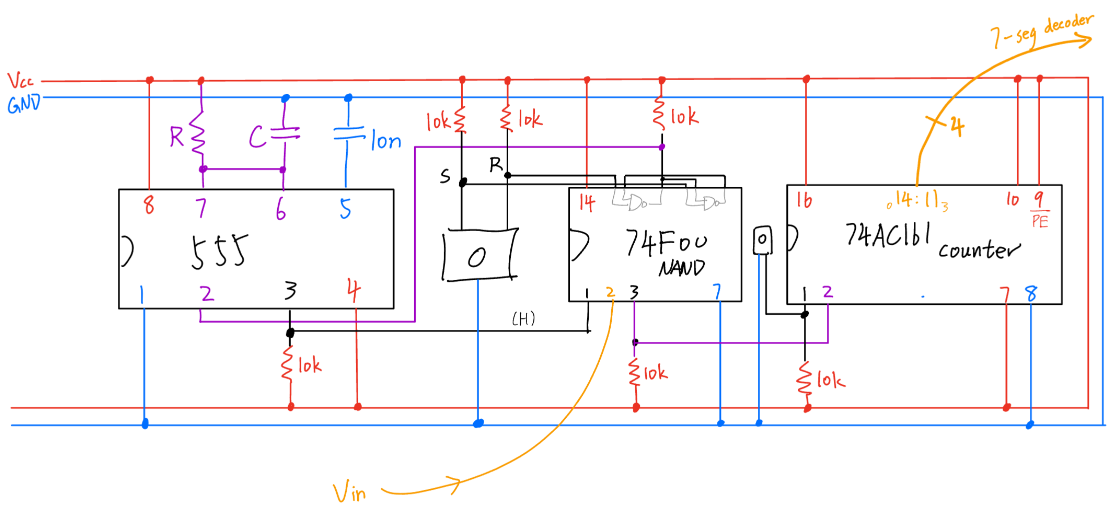
D. Frequency Counter

- Our 555 one-shot mode is configured to produce a 1-second high signal.
- We NAND it with a square wave from the function generator. During the interval, every falling edge of the input square wave will raise the NAND output.
- The NAND gate output is then fed as the CLK signal of the 74AC161 counter, which counts the number of rising edges (frequency), and outputs to the 7-seg decoder and display.
- When the one-shot output is low, the NAND gate will always output high, and the counter will not count.

Below is a block diagram:

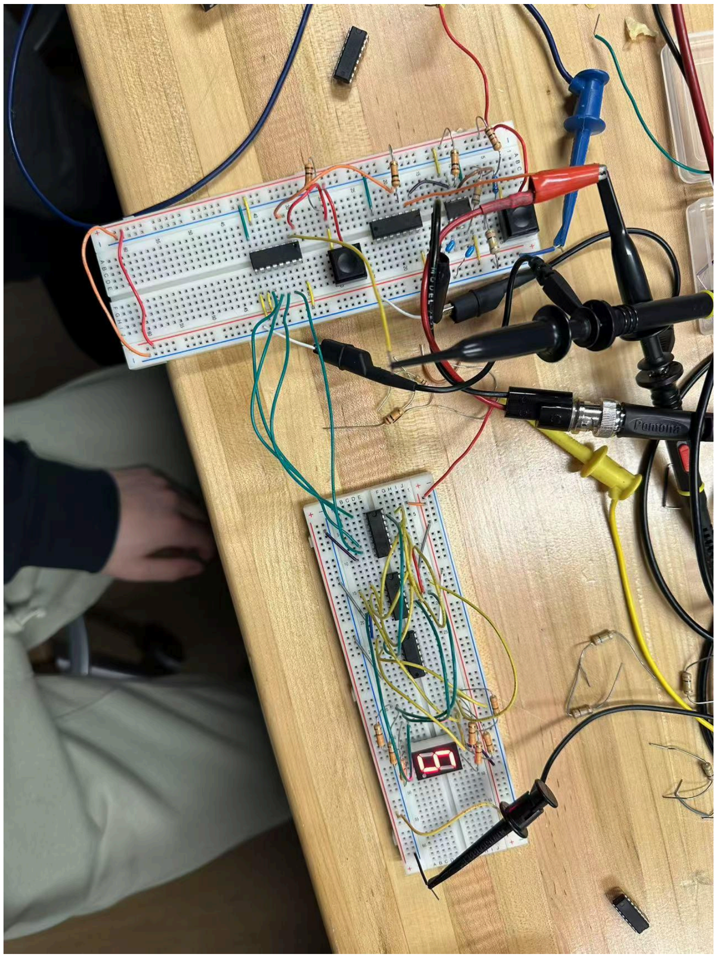


Below is the detailed wiring. Push buttons are used to start and reset the count.



Below is the result: we input a 5 Hz square wave sweeping from 0V to 5V, and the counter correctly counts 5 Hz.

- It may occasionally count 6 Hz, because it includes the falling edge of the one-shot.



There are no particular challenges for the counter design. The circuit is elegantly laid out. We did have some issues wiring the BCD-to-7-seg decoder, inverter, and display. (When debugging the circuits, we need to separate out different sections to test the functionality, which does cost some time). Those are some complicated wires.