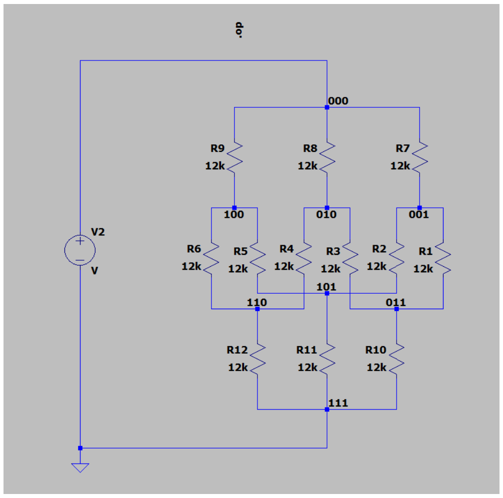
Part 1: DC Analysis

a. The cubic circuit is flattened into the diagram below, with the nodes labeled. I connected a 12V voltage source across the terminals. Below are the diagram and .op simulation results:

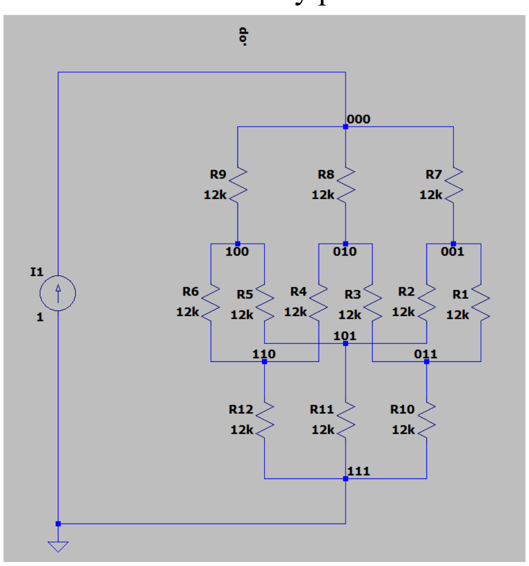



```
* C:\Users\13764\Documents\LTspice\Draft2.asc
       --- Operating Point ---

V(001):        7.2          voltage
V(011):        4.8          voltage
V(101):        4.8          voltage
V(010):        7.2          voltage
V(110):        4.8          voltage
V(100):        7.2          voltage
V(000):        12           voltage
I(R1):         0.0002       device_current
I(R2):         -0.0002      device_current
I(R3):         0.0002       device_current
I(R4):         -0.0002      device_current
I(R5):         0.0002       device_current
I(R6):         -0.0002      device_current
I(R7):         -0.0004      device_current
I(R8):         -0.0004      device_current
I(R9):         -0.0004      device_current
I(R10):        -0.0004      device_current
I(R11):        -0.0004      device_current
I(R12):        -0.0004      device_current
I(V2):         -0.0012      device_current
```

Using Ohm's Law, $R_{\text{eq}} = \frac{v_{v2}}{i_{v2}} = \frac{12\text{V}}{0.0012\text{A}} = 1\text{k}\Omega$.

Similarly, I drove the terminals with a 1A current source and measured the voltage across the current source. They produce the same results.

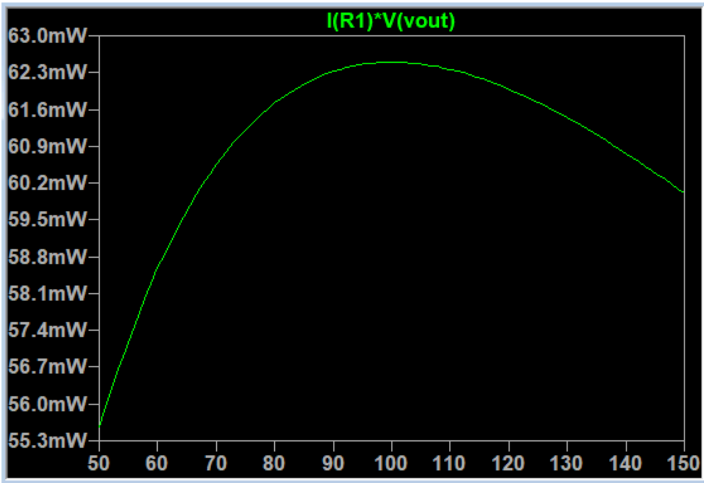



```
* C:\Users\13764\Documents\LTspice\Draft2.asc
       --- Operating Point ---

V(001):        6000         voltage
V(011):        4000         voltage
V(101):        4000         voltage
V(010):        6000         voltage
V(110):        4000         voltage
V(100):        6000         voltage
V(000):        10000        voltage
I(I1):         1            device_current
I(R1):         0.166667     device_current
I(R2):         -0.166667    device_current
I(R3):         0.166667     device_current
I(R4):         -0.166667    device_current
I(R5):         0.166667     device_current
I(R6):         -0.166667    device_current
I(R7):         -0.333333    device_current
I(R8):         -0.333333    device_current
I(R9):         -0.333333    device_current
I(R10):        -0.333333    device_current
I(R11):        -0.333333    device_current
I(R12):        -0.333333    device_current
```

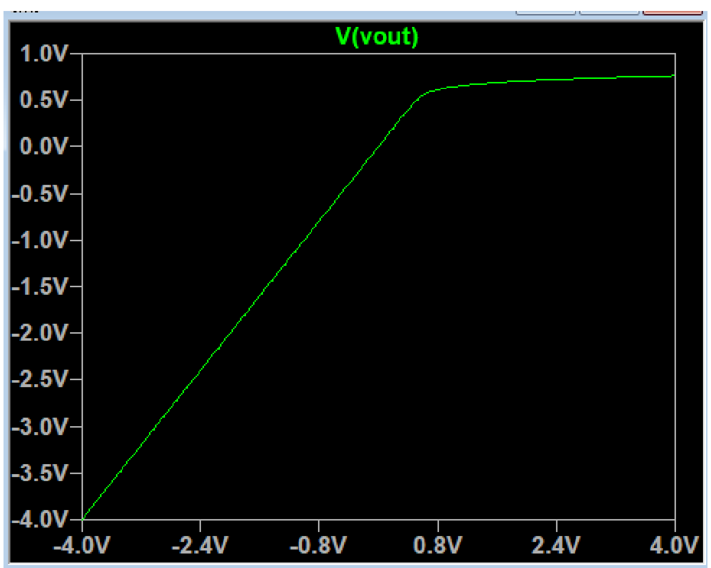
$$R_{\text{eq}} = \frac{v_{000} - 0}{i_{I1}} = \frac{10000\text{V}}{1\text{A}} = 1\text{k}\Omega.$$

b. P_{R1} = I(R1) * V(vout).



The shape is an upside-down curve, with a maximum at $R_{\text{load}} = 100\Omega$. If R_{load} is too low, most voltage will be wasted by R_2. If R_{load} is too high, less current will pass through the series circuit, decreasing the power. Since power is the product of voltage and current, the curve is bell-shaped, with a maximum occurring when $R_{load} = R_2$.

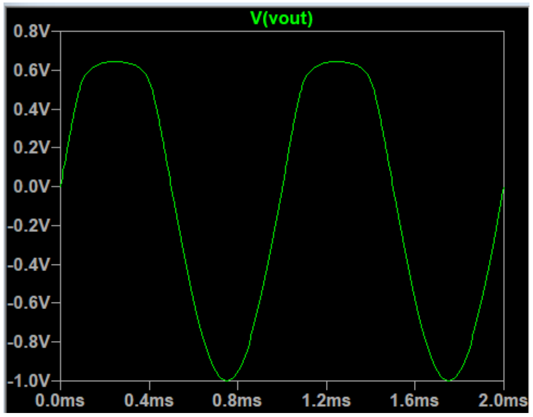
c. .dc Vin -4 4 0.01



At approximately Vin < 0.6 V, Vout = Vin. Once Vin > 0.6 V, Vout caps at 0.6 V. Therefore, the transfer curve is initially linear but flattens for positive Vin.

Part 2: Transient Analysis

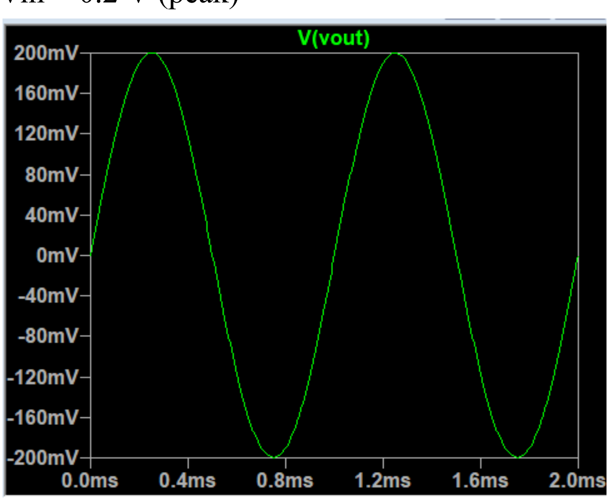
a. Vin = 1 V (peak)



Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	8.683e-1	1.000e+0	90.01°	0.00°
2	2.000e+3	9.565e-2	1.102e-1	0.10°	-89.90°
3	3.000e+3	5.249e-2	6.045e-2	89.75°	-0.26°
4	4.000e+3	1.638e-2	1.887e-2	-178.98°	-268.99°
5	5.000e+3	3.384e-3	3.898e-3	93.30°	3.30°
6	6.000e+3	8.331e-3	9.594e-3	178.89°	88.89°
7	7.000e+3	4.320e-3	4.975e-3	-90.41°	-180.42°
8	8.000e+3	1.727e-4	1.989e-4	133.94°	43.93°
9	9.000e+3	2.740e-3	3.156e-3	-85.15°	-175.15°
10	1.000e+4	1.473e-3	1.696e-3	-6.05°	-96.06°
11	1.100e+4	8.400e-5	9.674e-5	-81.91°	-171.91°
12	1.200e+4	8.053e-4	9.274e-4	-10.48°	-100.49°
13	1.300e+4	8.966e-4	1.033e-3	101.74°	11.74°
14	1.400e+4	3.753e-5	4.322e-5	36.63°	-53.38°
15	1.500e+4	4.292e-4	4.943e-4	94.86°	4.85°
16	1.600e+4	2.500e-4	2.879e-4	161.53°	71.53°
17	1.700e+4	5.501e-6	6.335e-6	-61.67°	-151.67°
18	1.800e+4	1.571e-4	1.809e-4	170.48°	80.48°
19	1.900e+4	1.391e-4	1.601e-4	-107.02°	-197.02°
20	2.000e+4	2.419e-5	2.786e-5	70.38°	-19.62°

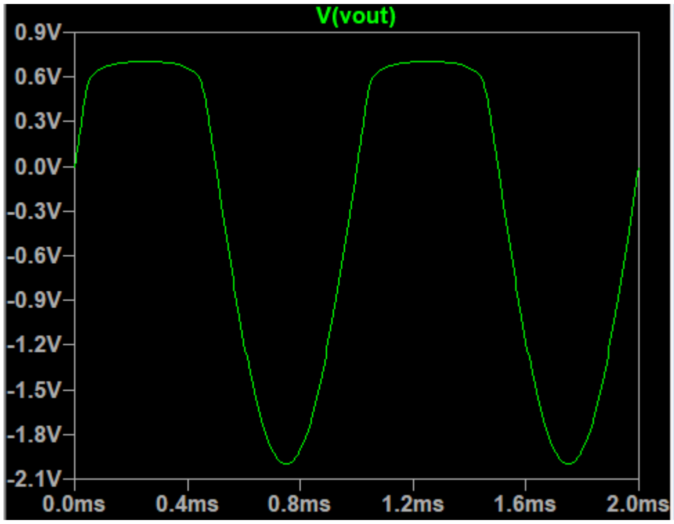
Partial Harmonic Distortion: 12.764093%
Total Harmonic Distortion: 12.764113%

Vin = 0.2 V (peak)



Partial Harmonic Distortion: 0.110740%
Total Harmonic Distortion: 0.111266%

Vin = 2 V (peak)

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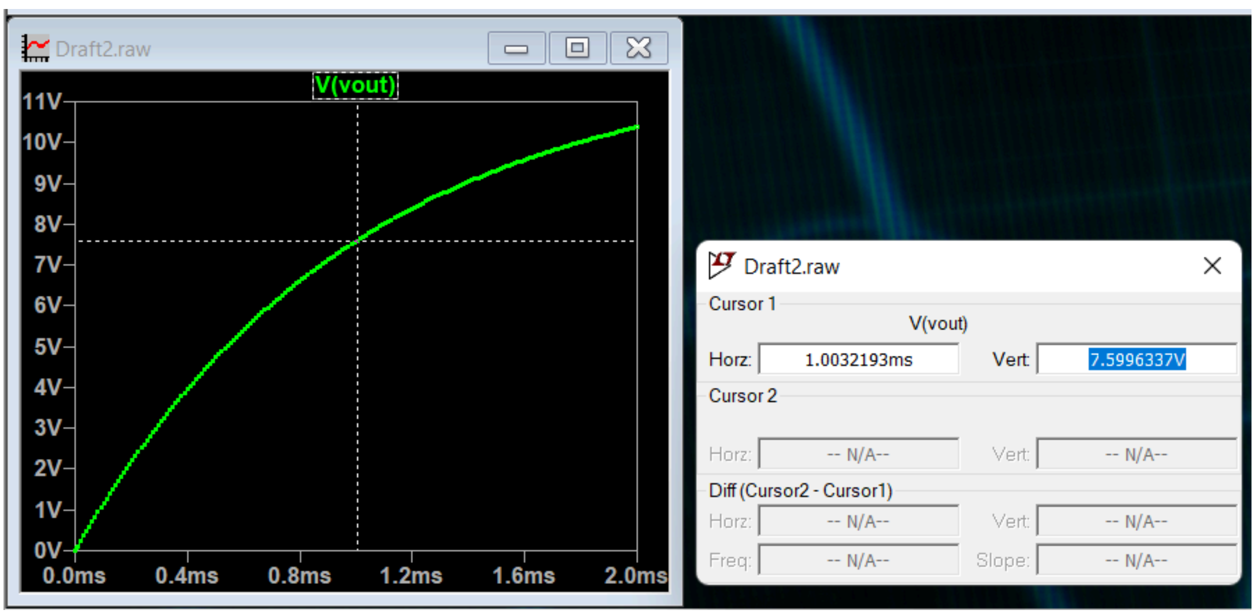
Partial Harmonic Distortion: 25.024182%
Total Harmonic Distortion:   25.024406%
```

The diode cuts off all the positive half of Vin and caps it at about 0.7 V. The higher the Vin peak, the more the distortion, as shown in the Fourier analysis.

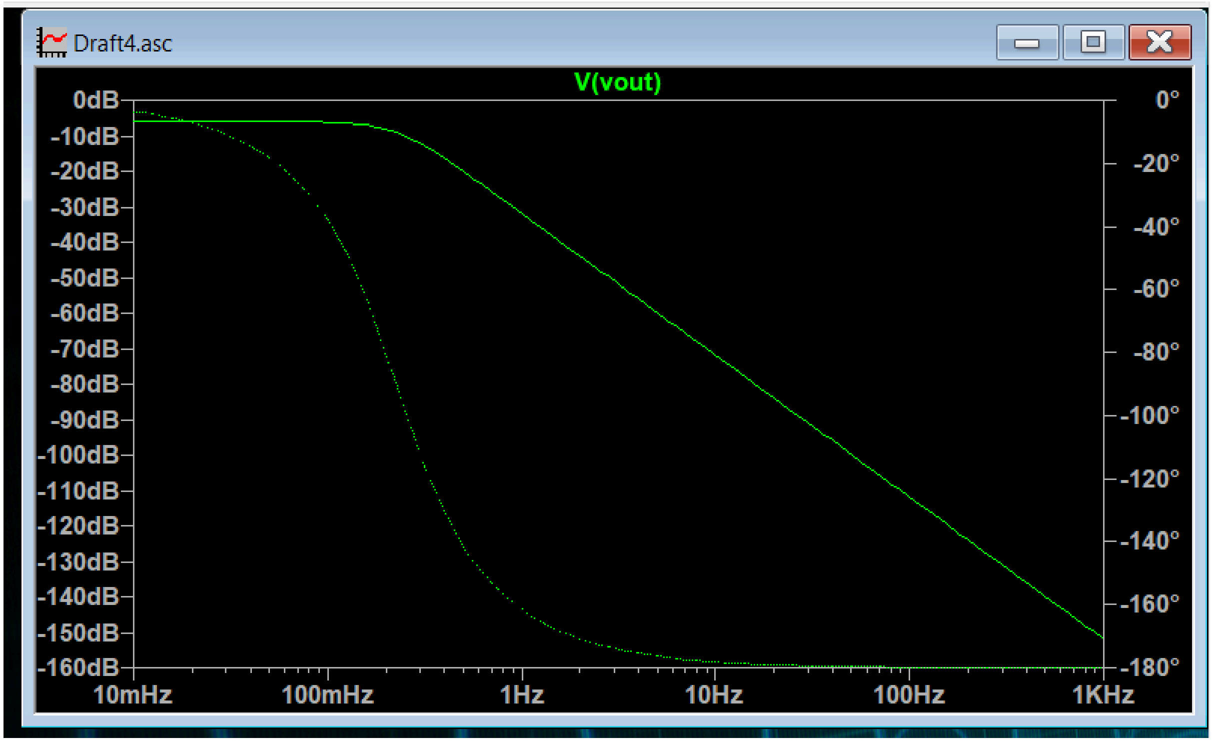
b.



The measured time constant is 1.00 ms.

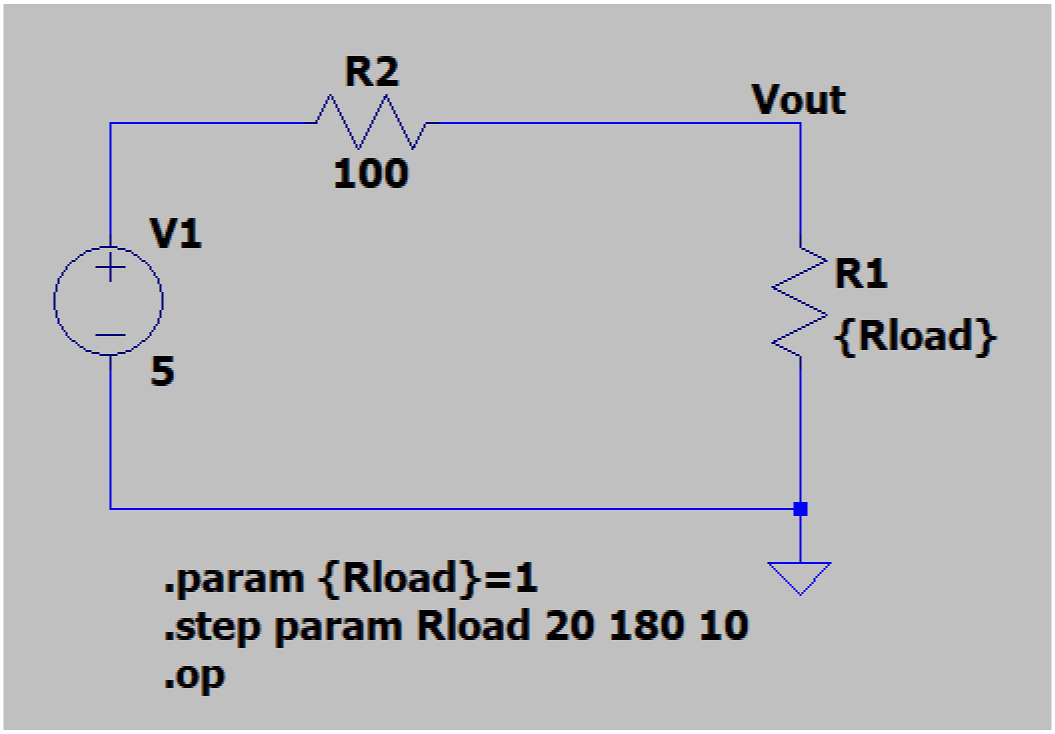
Part 3: AC Analysis

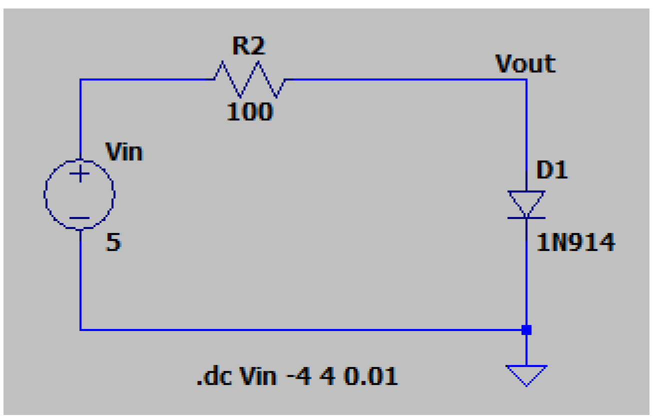
Trasient response plot:



The solid trace is the gain, and the dashed trace is the phase shift.

At low frequencies, the gain is relatively high, and there is almost no phase shift. At high frequencies, the gain drops significantly, almost close to 0. The phase shift is close to 180 degrees.
This is because, at low frequencies, the inductor has a low impedance (acts as a wire), while the capacitor has a high impedance (acts as a break). The circuit essentially divides Vin by half. At high frequencies, the L and C properties flip. Vout is almost shorted to the ground.


R2
100
Vout
V1
5
R1
{Rload}
.param {Rload}=1
.step param Rload 20 180 10
.op


R2
100
Vout
Vin
5
D1
1N914
.dc Vin -4 4 0.01